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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,423	11/11/2003	Dean A. Klein	MTIPAT.024C1	5166

20995 7590 06/28/2006

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EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,423	KLEIN, DEAN A.	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/11/03 & 2/16/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-40 are presented for examination.

2. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. The following is a quotation of 35 USC § 103 which forms the basis for all obviousness rejections set forth in this Office action: (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

(c) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

4. Claims 1, 9, 14-15, 24, 32 rejected under 35 USC § 102(b) as being clearly anticipated by Imamura et al., U.S. Patent 5,134,698.

Imamura et al. taught (e.g. see figs. 1-3) the invention as claimed (as per claim 1), including a data processing ("DP") system comprising:

A. a method of performing data string operations (col. 2 lines 23-27) comprising;

B. routing a series of instructions to a general purpose microprocessor (fig. 1, 1) having a first execution unit for executing instructions (unit 1 inherently contains an execution unit for executing instructions);

C. analyzing said series of instructions so as to detect an instruction to perform a data string operation (col. 5 lines 11-14, in order for the instruction to be transferred "from" the instruction processor, an "analysis" must have occurred to "detect" the instruction);

D. routing said instruction to perform a data string operation to a second execution unit (col. 5 lines 11-14, the instruction is sent "from" the instruction processor, which is a "routing") separate from said first execution unit (fig. 1, 2, storage controller 2 is separate from Instruction Processor 1), wherein said second execution unit receives an undecoded version of said instruction (fig. 2, col. 5 lines 19-30);

E. controlling read and write operations to and from external memory (fig. 1, 4, 5) with said general purpose microprocessor (1) via control circuitry (2), wherein said external

memory is external to said general purpose microprocessor (fig. 1, elements 4 and 5 are outside of element 1, therefore, are external to element 1);

F. controlling read and write operations to and from external memory (fig. 1, 4, 5) with said second execution unit via said control circuitry (col. 2 lines 23-41) and without intervention by said first execution unit (col. 7 line 62 to col. 8 line 2).

5. As to claim 9, it does not teach or define above the invention claimed in claim 1 and is therefore rejected under Imamura et al. for the same reasons set fourth in the rejection of claim 1, supra. As to the difference from claim 1, Imamura et al. taught that the memory circuitry (fig. 1, 4, 5) was external to the first and second execution units (2, 1) and that the first and second execution units were separately coupled to the memory circuits (fig. 1).

6. As to claim 14, it does not teach or define above the invention claimed in claim 9 and is therefore rejected under Imamura et al. for the same reasons set fourth in the rejection of claim 9, supra.

7. As to claim 15, it does not teach or define above the invention claimed in claim 1 and is therefore rejected under Imamura et al. for the same reasons set fourth in the rejection of claim 1, supra.

8. As to claim 24, it does not teach or define above the invention claimed in claim 1 and are therefore rejected under Imamura et al. for the same reasons set fourth in the rejection of claim 1, supra.

9. As to claim 32, it does not teach or define above the invention claimed in claim 1 and is therefore rejected under Imamura et al. for the same reasons set fourth in the rejection of claim 1, supra. Imamura et al. taught that the instruction was routed to the second execution unit for execution (col. 5 lines 11-14) and as such implicitly indicates that the instruction is not received by the first execution unit in the general purpose processor (1).

10. Claim 7-8, 10-13, 20-21, 38-40 are rejected under 35 USC § 103 as being unpatentable over Imamura et al., U.S. Patent 5,134,698, as applied to claims 1, 9, 14-15, 24, 32 , supra.

11. As to claim 7, Imamura et al. did not teach a cache. However, at the time of

applicant's invention, it was very well known to provide a cache for the purpose of enhancing performance of the system and official notice of such is hereby taken. Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have included a cache in any system built based upon the teachings of Imamura et al. because of this increased performance. Once one of skill in the art adds a cache to the system, it becomes inherent that the system must consult the cache for data to maintain memory coherency.

12. As to claim 8, once a cache is added to the system, it becomes inherent that modified data within that data cache will be flushed to main memory before or during the operation of a data string instruction in order to maintain memory coherency.

13. As to claim 10, it does not teach or define above the invention claimed in claim 7 and are therefore rejected under Imamura et al. for the same reasons set fourth in the rejection of claim 7, supra.

14. As to claim 11, caches inherently contain comparators to perform tag lookups, and therefore the addition of a cache to the Imamura et al. system would inherently include comparators.

15. As to claim 12, the cache lookup comparators inherently compare entries in a tag array with input addresses, and accordingly, would therefore be comparing addresses provided by both the first and the second execution units for accesses to memory lines stored in the cache.

16. As to claim 13, it does not teach or define above the invention claimed in claim 7 and is therefore rejected under Imamura et al. for the same reasons set fourth in the rejection of claim 7, supra. Furthermore, it is inherent that when a cache memory is present that a means be provided to maintain memory coherency.

17. As to claims 20-21, they do not teach or define above the invention claimed in claims 7-8 and are therefore rejected under Imamura et al. for the same reasons set fourth in the rejection of claims 7-8, supra.

18. As to claims 38-39, they do not teach or define above the invention claimed in claims 7-8 and are therefore rejected under Imamura et al. for the same reasons set fourth in the

rejection of claims 7-8, supra.

19. As to claim 40, Imamura et al. did not teach that the analyzing was performed by an instruction fetch unit. However, it is inherent that Imamura et al. system will contain an instruction fetch unit that fetches instructions. It is also inherent that a unit must perform the task of analyzing instructions to determine when to forward them to the second execution unit. Accordingly, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have the fetch unit perform the analysis and forwarding steps because a fetch unit must be present, and by having the fetch unit perform the analysis and forwarding steps the result would have been that the decoder of the first execution unit would have been simplified because it would not have had to concern itself with decoding instructions that were ultimately destined for a different execution unit in the system.

20. Claims 2-6, 16-19, 22, 25-31, 33-37 are rejected under 35 USC § 103 as being unpatentable over Imamura et al., U.S. Patent 5,134,698, as applied to claims 1, 9, 14-15, 24, 32, supra, in view of Young et al., U.S. Patent 5,548,730.

21. As to claim 2, Imamura et al. did not teach that the first and second execution units were on separate integrated circuits. However, Young et al. taught a separate integrated circuit containing a local processor circuit that was implemented as a separate integrated circuit (col. 2 lines 60-64, claim 1). As such, Young et al. is a teaching that it was well known to place secondary execution circuitry on a separate integrated circuit apart from the main processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to have placed the second execution unit of Imamura et al. on a separate integrated circuit apart from the instruction processor because of Young et al.'s teaching that doing such allows the second execution unit to perform tasks without interfering with the operations of the main processor (col. 4 lines 35-42, col. 5 lines 34-44).

22. As to claim 3, Young et al. taught that the second integrated circuit contained a bus interface unit (fig. 5, 120).

23. As to claim 4, Young et al. taught that the second integrated circuit contained a

memory controller (124).

24. As to claim 5, Imamura et al. taught that the data string instructions were routed to the second execution unit by writing the instructions to I/O addresses (col. 7 lines 24-35).

25. As to claim 6, Imamura et al. taught that the I/O addresses are inherently normally not used for I/O devices for the simple reason that if they were used for I/O devices, the data transferred to those addresses would arrive at those I/O devices, and not at the second execution unit.

26. As to claims 16-17, they do not teach or define above the invention claimed in claims 2-3 and are therefore rejected under Imamura et al. in view of Young et al. for the same reasons set fourth in the rejection of claims 2-3, supra.

27. As to claims 18-19, they do not teach or define above the invention claimed in claims 5-6 and are therefore rejected under Imamura et al. in view of Young et al. for the same reasons set fourth in the rejection of claims 5-6, supra.

28. As to claim 22, it does not teach or define above the invention claimed in claim 2 and is therefore rejected under Imamura et al. in view of Young et al. for the same reasons set fourth in the rejection of claim 2, supra.

29. As to claim 25-29, they do not teach or define above the invention claimed in claims 2-6 and are therefore rejected under Imamura et al. in view of Young et al. for the same reasons set fourth in the rejection of claims 2-6, supra.

30. As to claims 30-31, they do not teach or define above the invention claimed in claims 7-8 and are therefore rejected under Imamura et al. in view of Young et al. for the same reasons set fourth in the rejection of claims 7-8, supra.

31. As to claims 33-37, they do not teach or define above the invention claimed in claims 2-6 and are therefore rejected under Imamura et al. in view of Young et al. for the same reasons set fourth in the rejection of claims 2-6, supra.

32. Claim 23 is rejected under 35 USC § 103 as being unpatentable over Imamura et al., U.S. patent 5,134,698, as applied to claim 22, supra., in view of Groves, U.S. Patent

5,222,225.

33. As to claim 23, Imamura et al. did not teach that the host processing integrated circuit comprised both a general purpose execution unit and a dedicated string execution unit. However, Groves taught a host processing circuit composed of a general purpose execution unit and dedicated string execution unit (fig. 1). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have combined Groves disclosed system with that disclosed by Imamura et al. because of Groves teaching that his system provides an efficient method of manipulating character string data and provides for efficient storage of such character string data in memory (col. 2 line 66 to col. 3 line 3).

34. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

35. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (571) 272-4165. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (571) 272-4162. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Richard Ellis
June 21, 2006

RICHARD L. ELLIS
PRIMARY EXAMINER